REMARKS

Claims 1-23 are now present in this application.

Claims 1, 5, 10, 18, and 21-22 have been amended. Reconsideration of the application, as amended, is respectfully requested.

Rejection Under 35 U.S.C. 102(e)

Claims 1-9 and 18-23 stand rejected under 35 U.S.C. 102(e) as being anticipated by Foster et al., U.S. Patent 6,603,072). This rejection is respectfully traversed.

It is well established that a reference may anticipate a claim within the purview of 35 USC §102 only if all of the features and relationships recited in the claim are taught by the reference either by clear disclosure or under the principle of inherency. However, the patent to Foster et al. does not disclose all of the features recited in independent claim 1.

Independent claim 1 recites (emphasis added):

> 1. A dual chips stacked packaging structure, comprising:
> a first chip, having an active surface and an opposing non-active surface, the active surface consisting of a central area and a peripheral area having a plurality of first bonding pads;
> a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads;
> a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads, wherein ***the central area of the active surface of the first chip directly adheres to the first adhering surface of the chip paddle*** while an opposing central area of the opposing non-active surface of the second chip adheres to the second adhering surface of the chip paddle, and wherein the opposing central area of the opposing non-active surface of the second chip is opposite to the cent ral area of the active surface of the second chip; and

a plurality of wires, wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads.

In contrast, Foster et al. disclose a leadframe semiconductor package including multiple dies laminated in a stack with the die paddle of the leadframe being enhanced by laminating an "interposer" in the stack (see abstract) . The interposer comprises a laminate of at least one layer of a dielectric material and at least one layer of a metal that has been patterned to form a plurality of wire bonding pads arrayed around the periphery of one surface of the interposer. (see column 2, lines 52-56) The package 200 includes a metallic leadframe having a plurality of leads 202, semiconductor dies 206, a die paddle 204, wire bonds 208, and interposer 280. The leads 202 are arranged along the sides of a die paddle 204. The semiconductor dies 206 has wire bonding pads arrayed around a periphery of an active surface. The interposer 280 is laminated between the lower surface of the die paddle 204 and the upper surface of the lower die 206. The stack of dies 206, interposer 280, and die paddle 204 is laminated and wire bonded in sequential steps, with the upper die 106 being laminated and wire bonded last (see column 5, lines 9-20, and Fig. 2)

Foster et al. fails to teach or suggest that the central area of the active surface of the first chip **directly adheres to** the first adhering surface of the chip paddle, as is recited in independent claim 1. Instead, as disclosed by Foster et al. in column 5, lines 9-11 and Fig. 2, the interposer 280 is laminated between the lower surface of the die paddle 204 and the upper surface of the lower die 206.

Independent claims 5, 18 and 21 recite similar limitations, and are therefore the foregoing arguments in connection with independent claim 1 can also be applied to these claims.

It is therefore respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the structure of independent claims 1, 5, 18 and 21, and their dependent claims. Reconsideration and withdrawal of the 35 USC 102 rejection are respectfully requested.

Rejections Under 35 U.S.C. 103(a)

Claims 10-17 stand rejected under 35 USC 103 as being unpatentable over Foster et al. in view of Wu et al., U.S. Publication 2003/0214048. This rejection is respectfully traversed.

Independent claim 10 of the present application recites (emphasis added):

> 10. A dual chips stacked packaging structure, comprising:
> a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;
> a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;
> a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads, wherein ***the central area of the active surface of the first chip directly adheres to the first adhering surface of the chip paddle*** while an opposing central area of the opposing non-active surface of the second chip adheres to the second adhering surface of the chip paddle, and wherein the opposing central area of the opposing non-active surface of the second chip is opposite to the central area of the active surface of the second chip;
> a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and
> an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the non-active surface of the first chip and the total wire non-connecting surface of the leads exposed beyond the encapsulation.

Independent claim 10 recites that "the central area of the active surface of the first chip **directly adheres to** the first adhering surface of the chip paddle", which is similar to the limitations of claim 1 discussed above. Accordingly, the foregoing arguments in connection with independent claim 1 can also be applied to independent claim 10 and its dependent claims.

Furthermore, the secondary reference to Wu et al. fails to overcome the above-noted deficiencies of Foster et al.

The prior art utilized by the Examiner therefore fails to teach or suggest the structure of independent claim 10 and its dependent claims. Reconsideration and withdrawal of the 35 USC 103 rejection are respectfully requested.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: October 11, 2006

Respectfully submitted,

By _____
Joe McKinney Muncy
Registration No.: 32,334
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant